

Thermally Stable N-Metal Gate MOSFETs Using La-Incorporated HfSiO Dielectric

H.N. Alshareef¹, H.R. Harris², H.C. Wen, C.S. Park, C. Huffman¹, K. Choi, H.F. Luan³, P. Majhi⁴, B.H. Lee⁵, and R. Jammy⁵, D.J. Lichtenwalner⁶, J.S. Jur⁶, and A. I. King⁶

SEMATECH, 2706 Montopolis Drive, Austin, TX 78741. ¹Texas Instruments, ²AMD, ³Infineon, ⁴Intel, and ⁵IBM Assignees

⁶North Carolina State University, Department of Materials Science and Engineering, Raleigh, NC 27695
E-mail: Husam.alshareef@sematech.org

Abstract

We report a thermally stable N-metal process in which surface passivation of HfSiO dielectric using thin layers of La₂O₃, deposited by either MBE or PVD, significantly shifts the metal gate effective work function toward the Si conduction band edge. Well-behaved transistors with L_g down to 70 nm have been fabricated with threshold voltage of 0.25V, mobility up to 92% of the universal SiO₂ mobility, and T_{inv} ~1.6 nm.